Amendment to the Specification:

Please replace the paragraph [0024] with the following amended paragraph:

"Following that, referring to FIG. 2B, a photoresist layer (not shown in the figure) having open pattern formed on a surface of the second dielectric layer 211. Performing a photolithography and etching process to the photoresist layer in order to form the first opening 213 in the second dielectric layer 211 and the first dielectric layer 209, and exposing a portion of the surface of the ~~first dielectric layer 209~~ the polysilicon word lines 207. Then, forming an interim blanket titanium layer on the second dielectric layer 211, a side-wall and bottom of the first opening 213. Next, performing a rapid thermal annealing (RTA) process to convert the interim titanium layer to the first glue layer 215, for instance titanium/titanium nitride that utilizes to improve the adhesion with other metal layers, as shown in FIG. 2C."

Please replace the paragraph [0025] with the following amended paragraph:

"Subsequently, as shown in FIG. 2D, a first metal layer 217 is deposited on the surface of the first glue layer 215, for instance blanket tungsten that filled the first opening 213 and covered the surface of the first glue layer 215. Next, planarizing the first metal layer 217, for instance utilizing a method of chemical mechanical polishing or dry etching with conditions that have a higher ratio to tungsten and use the first glue layer 215 as an etch end point. Therefore, the surface of the first glue layer 215 and first opening 213, which is filled with the first metal layer 217, both are exposed. Then, a contact plug 216 is formed within the second dielectric layer 211 and the first dielectric layer 209, as shown in FIG. 2E."

Please replace the paragraph [0027] with the following amended paragraph:

"Next, referring to FIG. 2G, a patterned photoresist layer 219 is formed both on the surface of the second dielectric layer 211 and contact plug 216. Etching the photoresist layer 219 in order to form the second opening ~~211~~ 221 within the photoresist layer 219 and expose a portion of the second dielectric layer 211. In accordance with the position of the plurality of the buried bit lines 203, the second opening ~~211~~ 221 is placed between two of the plurality of

buried bit lines 203 and far away from the contact plug 216. After that, utilizing the photoresist layer 219 having the second opening 221 used as a mask to perform a ion implantation process 223 in the mask ROM device 200. The boron ions are implanted into the silicon substrate 201 through the second opening 221 within the photoresist layer 219 in order to form a plurality of code areas 224 in the silicon substrate 201, and between the two of the plurality of buried bit lines 203. The range of the implanted energy is about 200-1000 keV, preferably is about 300 keV."